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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,855	03/30/2004	Hannu Ventomaki	915-007.083	5601

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EXAMINER	
NGUYEN, JIMMY	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,855	VENTOMAKI, HANNU	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Argument

The amendment filed 6/13/05 has been carefully considered with the following effect;

First, the applicants fail to respond to the claim objection as indicated in the previous office action which is claims 1 – 12 are lacking the method step.

Second, in claim 13 instead of the apparatus claim, the applicants are listing the method step.

Third, the newly added limitation " said support elements are electrically connected to each other on the side of the IC package" does not overcome the previous office action because if the support element are electrically connected to each other that means the support elements have electrical characteristic (conducting electrical signal from one place to another); therefore these support elements are nothing but IC pins that insert to the printed circuit board and analyzing for the connection.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 –28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 – 12 are lacking the method step.

Claims 13 – 28 are lacking the apparatus claims.

Correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Rampone et al (US 5,966,020).

As to claim 1, Rampone et al disclose a method for analyzing connection conditions between an integrated circuit package (180, fig 2) and a circuit board (230, fig 5),

- wherein said integrated circuit package (180, fig 2) is electrically coupled to said circuit board (230, fig 5) by coupling elements (290, 291, fig 5), and

wherein said integrated circuit package (180, fig 2) is mechanically connected with said circuit board (230, fig 5) by support elements (270, 271, 260, 261, 315, 335, and IC pins), characterized in that said support elements (IC pins) are electrically connected to each other on the side of the IC package (180)

physical values are picked-off from said support elements (315, 335, fig 7), and said physical values are evaluated (by the probes 400, 420) to determine the condition of said connection between said integrated circuit package (180, fig 2) and said circuit board (230, fig 5).

As to claim 2, Rampone et al disclose the electrical values are pick off from support elements (315, 335, fig 7).

As to claim 3, Rampone et al disclose the electrical current (column 6 lines 55 – 60) within the support element is picked off (315, 335, fig 7).

As to claims 4, 5, Rampone et al disclose the mechanical values (the joint solder are making sure the pins are connected) are picked off from support elements (270, 271, 260, 261, 315, 335) by using the strain gauge (probe, 40, 420).

As to claim 6, Rampone et al disclose a condition of electrical coupling of IC package (180, fig 2) with circuit board (230) is concluded form determined condition of connection.

As to claim 7, Rampone et al disclose the connection condition is determined in intervals (step 515 of fig 8).

As to claims 8 – 12, 22, 24 – 26, Rampone et al disclose determined connection condition is determined , store and presented on a user interface , a error message is generated (all of the this from the tester, not shown which is connected to probes 400, 420).

As to claims 13, 27, Rampone et al disclose a system for analyzing connection conditions between an integrated circuit package (180, fig 2) and a circuit board 230, fig 5) comprising:

coupling elements (290, 291, fig 2) coupling said integrated circuit package (180, fig 2) electrically to said circuit board (230, fig 5), and

support elements (270, 271, 260, 261, 315, 335) connecting said integrated circuit package (180, fig 2) mechanically with said circuit board (230, fig 5),

characterised by

electrically connecting support elements (270, 271, 260, 261, 315, 335, and IC pins), on the side of the IC package (180)

measuring (by probes 400, 420, fig 7) means arranged at said support elements (315, 335) to pick-off physical values from said support elements, and

evaluation means evaluating said physical values to determine the condition of said connection between IC package (180, fig 2) and circuit board (230, fig 5).

It is noted that the preamble of claim 27 is not given any patentable weight.

As to claim 14, Rampone et al disclose the support elements (270, 271, 260, 261, 315, 335) are arranged between circuit board (230, fig 5) and IC package (180, fig 2).

As to claim 15, Rampone et al disclose the support elements are solder pads elements (270, 271, 260, 261, 315, 335)

As to claim 16, Rampone et al disclose the support elements (270, 271, 260, 261, 315, 335) are arranged adjacent to coupling elements (290, 291).

As to claim 17, Rampone et al disclose the support elements (270, 271, 260, 261, 315, 335) are arranged semicircular along coupling elements (290, 291).

As to claim 18, Rampone et al disclose the support elements (270, 271, 260, 261, 315, 335) are arranged along edges and or at corners of IC package (180, fig 2).

As to claim 19, Rampone et al disclose IC package is a CSP of chip (180, fig 2).

As to claims 20, 21, Rampone et al disclose the means of measuring electrical and mechanical condition of support element (270, 271, 260, 261, 315, 335).

As to claim 23, Rampone et al disclose the evaluation means compare picked off physical values with comparative values to determine the connection condition (step 515 of fig 8)

As to claims 28, 29, Rampone et al disclose the ATE system (column 6 lines 30) which is connect to the probes (400,420), therefore it is inherently that the computer program operable to cause a processor to analyze connection condition beween an IC and circuit board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571 – 272-1965. The examiner can normally be reached on Monday - Friday from 9am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramiz Nestor, can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

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JN.
August 9, 2005